

CLAIMS

What is claimed is:

- 1) A method for reducing power in MRAM comprising:
 - 2 (a) storing information in a RAM buffer;
 - 4 (b) reading the information from the RAM buffer;
 - 6 (c) writing the information to the MRAM;
 (d) such that all storage cells connected to a selected wordline in the MRAM
 are written.

- 2) The method in Claim 1 wherein the RAM buffer is an SRAM buffer.

- 3) The method in Claim 1 wherein the RAM buffer is a DRAM buffer.

- 4) The method in Claim 1 wherein the RAM buffer is an array of flip-flops.

- 5) A method for reducing power in MRAM comprising:

- 2 (a) storing information from N write cycles in a RAM buffer;
- 4 (b) reading the information from the RAM buffer using fewer than N read
 cycles;
- 6 (c) writing the information to the MRAM using fewer than N write cycles;

6 (d) such that the number of power-up sequences required to write the
information to the MRAM is reduced.

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6) The method in Claim 5 wherein the RAM buffer is an SRAM buffer.

2

7) The method in Claim 5 wherein the RAM buffer is a DRAM buffer.

2

8) The method in Claim 5 wherein the RAM buffer is an array of flip-flops.

2

9) A method for reducing power in MRAM comprising:

2 (a) storing information from N write cycles in a RAM buffer;
4 (b) reading the information from the RAM buffer using one read cycle;
4 (c) writing the information to the MRAM using one write cycle;
6 (d) such that only one power-up sequence is used to write the information to
the MRAM.

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10) The method in Claim 9 wherein the RAM buffer is an SRAM buffer.

2

11) The method in Claim 9 wherein the RAM buffer is a DRAM buffer.

2

12) The method in Claim 9 wherein the RAM buffer is an array of flip-flops.

2

13) A system for reducing power in MRAM comprising:

2

(a) a RAM buffer;

(b) a MRAM;

4

(c) wherein the RAM buffer stores information;

(d) wherein the information stored in the RAM buffer is written to the MRAM

6

such that all storage cells connected to a selected wordline in the MRAM

are written.

8

14) The system in Claim 13 wherein the RAM buffer is an SRAM buffer.

2

15) The system in Claim 13 wherein the RAM buffer is a DRAM buffer.

2

16) The system in Claim 13 wherein the RAM buffer is an array of flip-flops.

2

17) A system for reducing power in MRAM comprising:

2

(a) a RAM buffer;

(b) a MRAM;

4

(c) wherein the RAM buffer stores information for N cycles;

(d) wherein the information stored in the RAM buffer is written to the MRAM

6 in less than N cycles;

(e) wherein the number of power-up sequences required to write the

8 information to the MRAM is reduced.

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18) The system in Claim 17 wherein the RAM buffer is an SRAM buffer.

2

19) The system in Claim 17 wherein the RAM buffer is a DRAM buffer.

2

20) The system in Claim 17 wherein the RAM buffer is an array of flip-flops.

2

21) A system for reducing power in MRAM comprising:

2 (a) a RAM buffer;

4 (b) a MRAM;

4 (c) wherein the RAM buffer stores information for N cycles;

6 (d) wherein the information stored in the RAM buffer is written to the MRAM

6 in one cycle;

8 (e) wherein only one power-up sequence is required to write the information

8 to the MRAM.

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22) The system in Claim 21 wherein the RAM buffer is an SRAM buffer.

2

23) The system in Claim 21 wherein the RAM buffer is a DRAM buffer.

2

24) The system in Claim 21 wherein the RAM buffer is an array of flip-flops.

2

25) A system for reducing power in MRAM comprising:

2 (a) a means for electronically reading and writing information;

4 (b) a MRAM;

4 (c) wherein the means for electronically reading and writing information
 stores information for N cycles;

6 (d) wherein the information stored in the means for electronically reading and
 writing information is written to the MRAM in less than N cycles;

8 (e) wherein the number of power-up sequences required to write the
 information to the MRAM is reduced.

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